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HfO_x-Based Vertical Resistive Switching Random Access Memory Suitable for Bit-Cost-Effective Three-Dimensional Cross-Point Architecture

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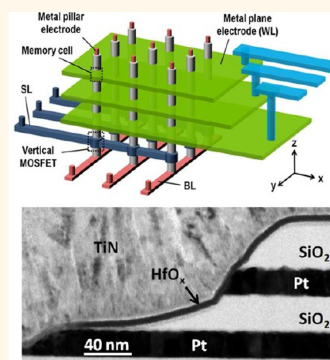
ABSTRACT The three-dimensional (3D) cross-point array architecture is attractive for future ultra-high-density nonvolatile memory application. A bit-cost-effective technology path toward the 3D integration that requires only one critical lithography step or mask for reducing the bit-cost is demonstrated in this work. A double-layer HfO_x-based vertical resistive switching random access memory (RRAM) is fabricated and characterized. The HfO_x thin film is deposited at the sidewall of the predefined trench by atomic layer deposition, forming a vertical memory structure. Electrode/oxide interface engineering with a TiON interfacial layer results in nonlinear $I-V$ suitable for the selectorless array. The fabricated HfO_x vertical RRAM shows excellent performances such as reset current (<50 μA), switching speed (<100 ns), switching endurance (>10^8 cycles), read disturbance immunity (>10^9 cycles), and data retention time (>10^5 s @ 125 °C).



KEYWORDS: resistive switching · RRAM · cross-point array · HfO_2 · bit-cost-effective · 3D integration

Resistive switching random access memory (RRAM) is one of the most promising candidates for future nonvolatile memory application.[1,2] The electrically triggered resistance switching phenomenon has been observed in dozens of materials, including amorphous silicon,[3] amorphous carbon,[4] chalcogenide,[5] and oxides such as NiO,[6] TiO_x,[7] WO_x,[8] HfO_x,[9,10] TaO_x,[11] and AlO_x.[12] Among these materials, the oxide-based RRAM has shown attractive performances including fast switching speed (~ns[9]), excellent scalability (<10 nm cell size[10]), long endurance (>10^{12} cycles[11]), and stable data retention at elevated temperature (>10 years extrapolated[9−11]), along with compatibility with the complementary metal-oxide-semiconductor (CMOS) technology. In addition, Mb-size array with CMOS peripheral circuits has been demonstrated in HfO_x RRAM.[13] However, the RRAM technology has not yet begun to replace the mainstream commercialized FLASH technology even though RRAM has shown better switching speed and endurance than FLASH technology. In addition to the challenges from device physics such as variability control,[14] a key challenge for RRAM is improving the integration density in terms of cost per bit (bit-cost), so it can compete with the multibit storage NAND FLASH. State-of-the-art NAND FLASH has been scaled down to the sub-20 nm regime,[15] and the three-dimensional (3D) stackable NAND FLASH is emerging.[16−19] To achieve similar device density to the 3D NAND FLASH, a technology path toward the 3D stackable RRAM is required. There are two 3D integration approaches available: one is the conventional planar RRAM-based cross-point array[20,21] stacked layer by layer; the other one is the novel vertical RRAM[22,23] sandwiched between the pillar electrodes and multilayer plane electrodes. The first approach using simply stacked planar RRAM does not save lithography steps or masks, and therefore the bit-cost remains high. The second approach, using vertical RRAM, requires only one critical lithography step or mask; thus it is a more promising approach for reducing the bit-cost. In this work, we demonstrate the

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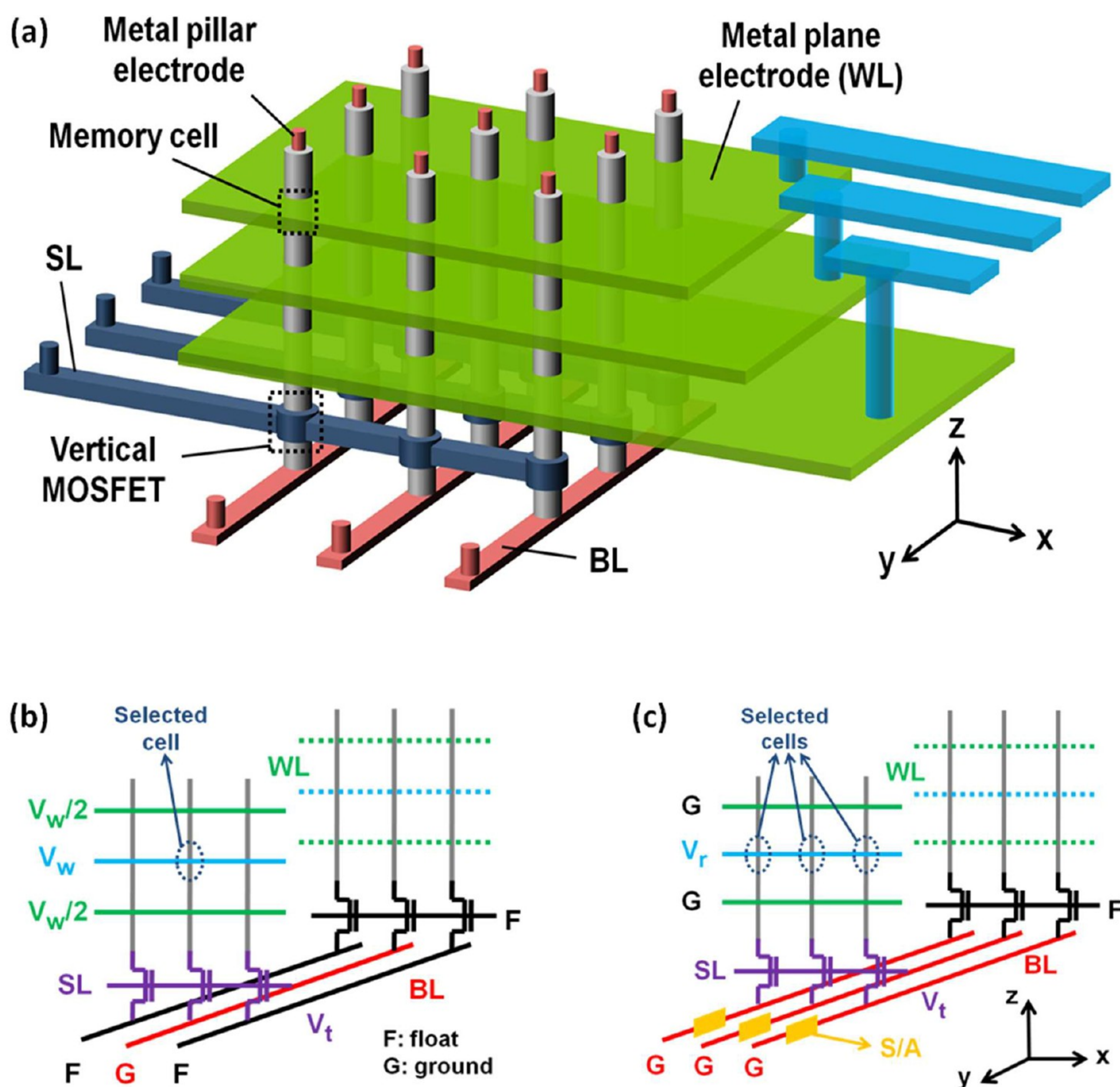

Figure 1. (a) Schematic of the proposed 3D cross-point architecture using the vertical RRAM cell demonstrated in the work. The vertical RRAM cells are formed at the intersections of each pillar electrode and each plane electrode: the resistive switching oxide layer surrounds the pillar electrode and is also in contact with the plane electrode. To enable the random access of each memory cell, three-dimensional decoding is needed through WL (decoding in the *z*-direction), BL (decoding in the *y*-direction), and SL of the gate of the vertical MOSFET (decoding in the *x*-direction). (b) Biasing diagram for the write operation. During the write operation, a specific cell is selected: write voltage (Vw) is applied on the selected cell's WL, and Vw/2 is applied on all the unselected cells' WL to avoid unintentional writing. To select the pillar where the selected cell is located, the SL of that pillar is turned on and the corresponding BL is grounded. (c) Biasing diagram for the read operation. During the read operation, a row of cells (on the same SL line) on one plane is read out simultaneously: read voltage (Vr) is applied on the selected cells' WL, the SL that controls the selected cells is turned on, and the data of a row of cells are read out by the sense amplifiers (S/A).

bit-cost-effective vertical RRAM concept in HfO_x, which is one of the most explored and relatively more mature resistive switching material systems so far.[9,10,24] Excellent device performances are obtained in the fabricated HfO_x vertical RRAM, showing the potential for 3D integration. Furthermore, we propose a 3D cross-point architecture with three-dimensional decoding strategy (by the plane electrode word lines, by the bit lines, and by the select lines) to enable the individual cell random access, and we discuss the corresponding write/read operation schemes, both of which were not explicitly discussed in the previous works.[22,23]

The mechanism of the resistive switching phenomenon in oxides has been widely attributed to the formation/rupture of the nanoscale conductive filaments, which may consist of oxygen vacancies.[25] The transition from high resistance state (HRS) to low resistance state (LRS) is called the SET process, while the transition from LRS to HRS is called the RESET process. The SET process is interpreted as a dielectric soft breakdown associated with the migration of oxygen ions toward one electrode, leaving behind the conductive filaments in the bulk oxide. In the bipolar RESET mode, the reserved electric field and Joule heating assist the oxygen ions' migration from the electrode/oxide interface reservoir, and they can recombine with the oxygen vacancies, thus partially rupturing the conductive filaments. For more

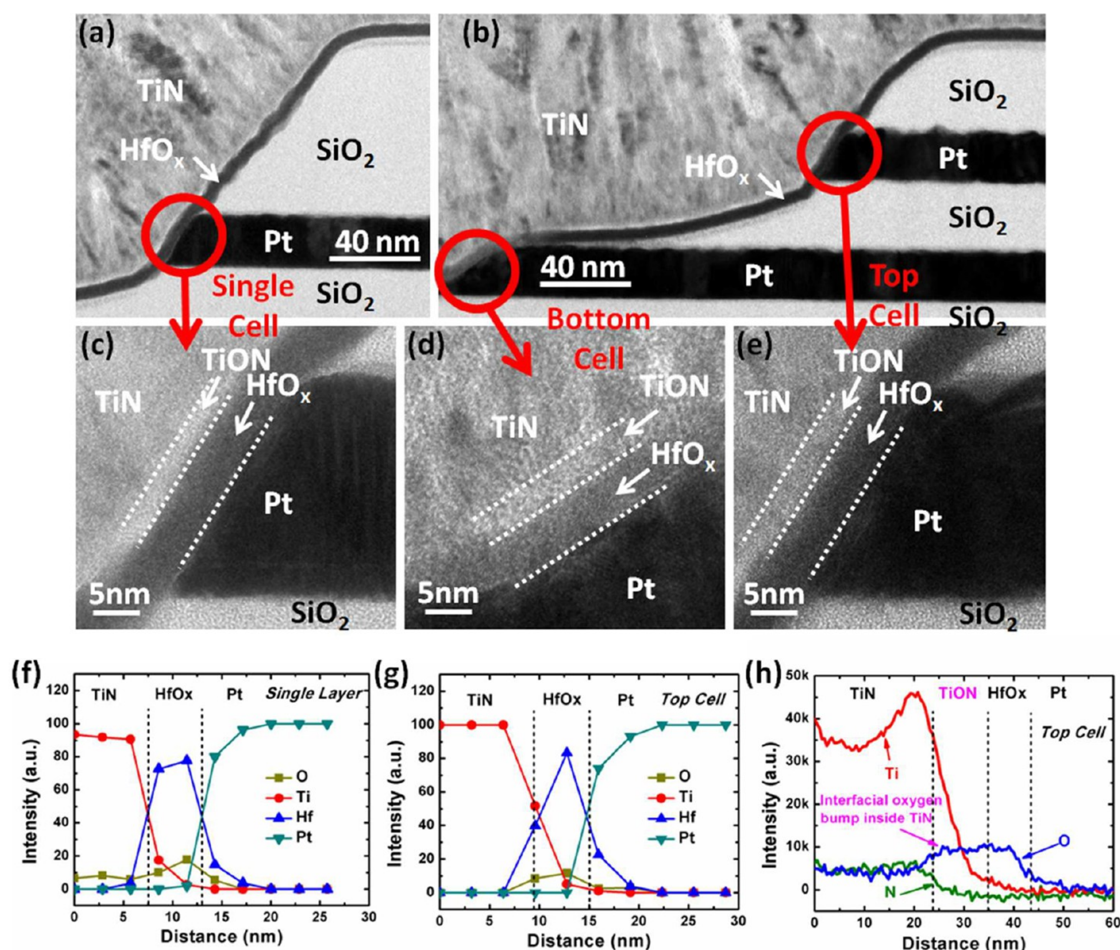

Figure 2. Cross-section TEM of (a) the single-layer sample and (b) the double-layer sample; HR-TEM of (c) the cell in the single-layer sample, (d) the bottom cell, and (e) the top cell in the double-layer sample. The TiN pillar electrode, TiON interfacial layer, HfO_x resistive switching layer, and Pt plane electrode are clearly shown. EDX composition profile through the sidewall of the cell in (f) the single-layer sample and (g) the top cell in the double-layer sample. EELS composition profile through the sidewall of (h) the top cell. Oxygen bump shows up at the TiN/HfO_x interface, suggesting the formation of an interfacial TiON layer, which may cause an electron tunneling barrier and a nonlinear *I*−*V* curve for the RRAM cell.

discussions on the switching mechanism, please refer to the work in ref 26.

RESULTS AND DISCUSSION

We propose a 3D cross-point memory architecture with $4F^2/m$ cell size (*F* is the lithography feature size, *m* is the number of stacked layers), enabling the random access of individual memory cells. Figure 1a shows the schematic of our proposed structure. The vertical RRAM cells are formed at the intersections of each pillar electrode and each plane electrode (acting as the word-line, WL): the resistive switching oxide layer surrounds the pillar electrode and is also in contact with the plane electrode. To enable the random access of each memory cell individually, which is a key distinguishing feature of RRAM as compared to FLASH, three-dimensional decoding is needed. We propose using a vertical MOSFET (*e.g.*, the gate-all-round silicon vertical nanowire transistor[27]) to serve as bit-line (BL) selector, whose gate is controlled by the select-line (SL). With the appropriate bias schemes on the WL (decoding in the *z*-direction), BL (decoding in the *y*-direction), and SL (decoding in the *x*-direction), each memory cell in the 3D cross-point architecture can be individually accessed. The biasing diagram for the write operation is shown in Figure 1b, and that for the read operation is shown in Figure 1c. During the write operation, a specific cell is selected: write voltage (Vw) is applied on the selected cell's WL, and Vw/2 is applied on all the unselected cells' WL to avoid unintentional writing. To select the pillar where the selected cell is located, the SL of that pillar is turned on and the corresponding BL is grounded. During the read operation, a row of cells (on the same SL line) on one plane is read out simultaneously: read voltage (Vr) is applied on the selected cells' WL; SL that controls the selected cells is turned on, and the data of a row of cells are read out by the sense amplifiers.

As a proof-of-concept work, we design a bit-cost-effective fabrication process for the potential 3D integration (see the Methods Section) and demonstrate a single-layer and double-layer HfO_x-based vertical

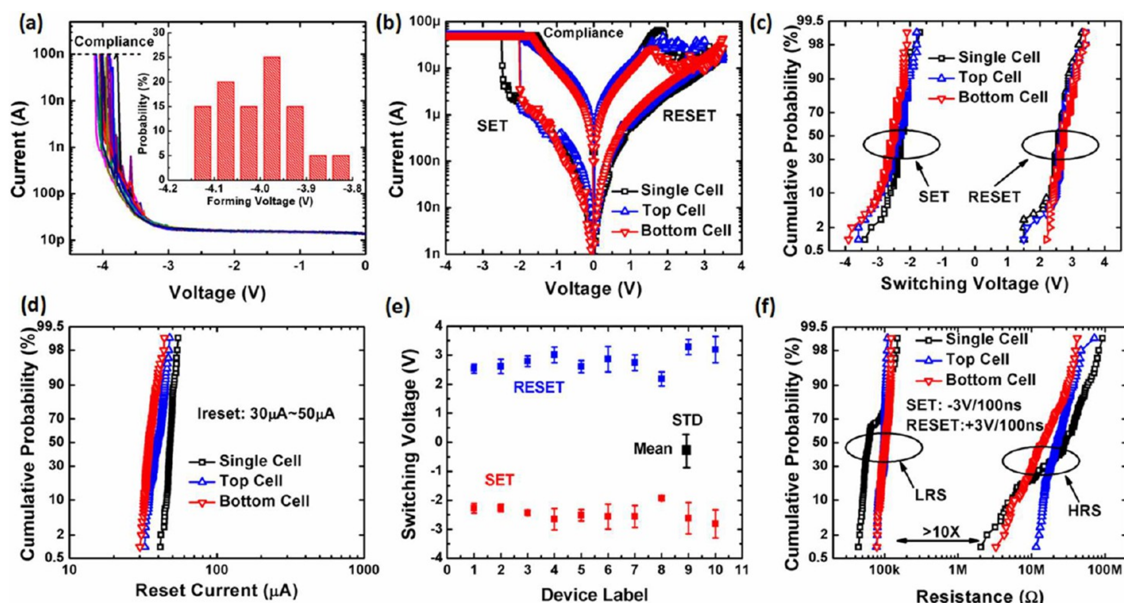

Figure 3. Statistics of the vertical HfO_x RRAM's switching characteristics. (a) Forming process measured from 20 different cells (100 nA compliance is applied). Inset: Forming voltage distribution of ~4 V. (b) Direct current *I*−*V* bipolar switching characteristics (50 μA compliance current is applied). (c) Switching voltage distribution (average ~3 V) by hundreds of continuous sweep cycles. (d) Reset current distribution by hundreds of continuous sweep cycles with an average of <50 μA. (e) Switching voltage distribution collected from 10 different cells. (f) Resistance distribution obtained by hundreds of continuous pulse cycles. LRS resistance is ~100 kΩ with a HRS/LRS resistance window of >10×. Consistent switching characteristics exisit among cells in the single-layer sample and top cell and bottom cell in the double-layer sample. The reasonably controlled device-to-device variation suggests the potential of stacking even more layers.

RRAM. First, the cross-sectional topology characterization of the fabricated devices is performed. Figure 2a and b show the transmission electron microscopy (TEM) image of the single-layer sample and the double-layer sample, respectively. Figure 2c−e show the high-resolution TEM (HR-TEM) image of the cell in the single-layer sample and the top cell and bottom cell in the double-layer sample. A TiN/TiON/HfO_x/Pt stack is observable in the TEM image analysis. It is noted that the trench is not perfectly sharp due to the limited etching capability in our university-grade fabrication facility. Second, the materials composition characterization of the fabricated devices is performed. Figure 2f and g show the composition spatial profile through the sidewall of the single-layer sample and double-layer sample by energy-dispersive X-ray spectroscopy (EDX). The TiN pillar electrode, HfO_x resistive switching layer, and Pt plane electrode are clearly shown in this spatial profile. We are also interested in the electrode/oxide interface property since it is known to affect the resistive switching behavior.[28] The electron energy loss spectroscopy (EELS) analysis is performed at the interface between TiN and HfO_x as shown in Figure 2h: an oxygen bump appears at the interface, suggesting the formation of an interfacial TiON layer. This interfacial layer may cause an electron tunneling barrier for the RRAM device and results in a nonlinear *I*−*V* curve, as we shall see next in the device electrical characterization.

In the following, we characterize the fabricated vertical HfO_x RRAM electrical properties. First, the statistics of the device performances such as the switching voltage, the reset current, and the HRS and LRS resistances are measured. Figure 3a shows the forming process for 20 different cells: the as-fabricated devices usually need ~4 V forming voltage to trigger the switching from the initial resistance state to LRS and initiate the subsequent switching cycles. Figure 3b shows the typical dc *I*−*V* curves of the single-layer sample and the top cell and bottom cell in the double-layer sample. A compliance current of ~50 μA is enforced by the semiconductor parameter analyzer to avoid damaging the cell during the abrupt SET process. Figure 3c shows the switching voltage distribution, which has an average of ~3 V. Figure 3d shows the reset current distribution with an average less than 50 μA. Figure 3e shows the device-to-device statistics of the switching voltage from 10 different cells, showing a reasonably controlled variation and reproducibility. These statistically measured results show consistent switching characteristics among the single-layer sample and the top cell as well as the bottom cell in the double-layer sample, thus suggesting the potential of stacking multilayer vertical RRAM using this cost-effective fabrication process. Figure 3f shows the distribution of the programmed resistance value obtained by hundreds of pulse cyclings with ±3 V/100 ns programming condition. It is seen

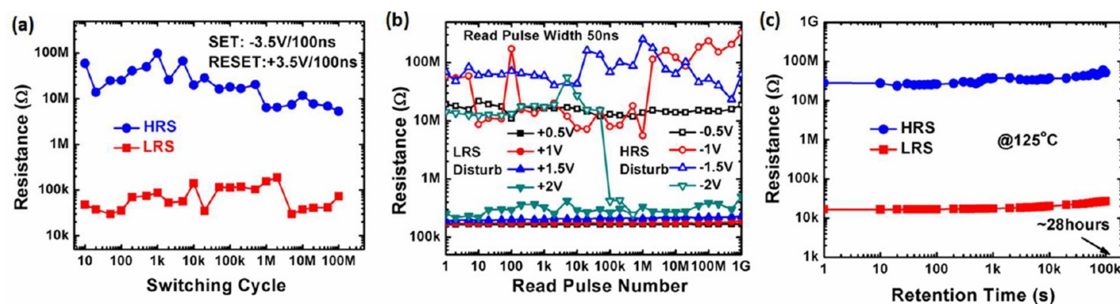

Figure 4. Reliability test of the vertical HfO_x RRAM device performed on the single-layer sample. (a) Switching endurance test. The device can switch $>10^8$ cycles under ± 3.5 V/100 ns write pulse conditions. (b) Read disturbance test. The device can maintain its states for $>10^9$ cycles under ± 1.5 V/50 ns read pulse conditions. (c) Data retention test. The device can maintain its states for $>10^5$ s (~28 h) @ 125 °C.

that the average LRS resistance is ~100 kΩ, and the HRS/LRS resistance window maintains >10×. The measured ~100 kΩ LRS resistance is larger than the previously reported ~10 kΩ resistance in HfO_x RRAM devices,[9,12,24] and the origin of this increased LRS resistance is attributed to the TiON interfacial layer, as observed in the EELS analysis in Figure 2h. This hypothesis is further supported by the LRS conduction mechanism study. The weak dependence of the LRS current on temperature (see Supporting Information S1) suggests that the conduction in LRS is dominated by electron tunneling through an interfacial barrier. As a result, the LRS resistance is effectively raised to ~100 kΩ. Finally, the reliability of the fabricated devices is examined. Figure 4a shows that $>10^8$ switching endurance cycles can be achieved with ±3.5 V/100 ns pulse conditions. Figure 4b shows that $>10^9$ read disturbance immunity cycles can be achieved up to ±1.5 V/50 ns pulse conditions. Figure 4c shows that a $>10^5$ s data retention time can be obtained at 125 °C. The measured reliability suggests that the HfO_x vertical RRAM is reliable for nonvolatile memory application.

The increased LRS resistance is beneficial for realizing the cross-point memory architecture without an explicit cell selector, because the array size is mainly limited by the ratio between the interconnect resistance and the memory LRS resistance.[29] A relatively large LRS resistance is helpful to reduce the voltage drop on the interconnect and mitigating the sneak path leakage current. To support this claim, we perform a SPICE simulation on the 3D cross-point architecture with the device characteristics demonstrated and the write/read scheme proposed in this work. The simulation results suggest that an up to Mb scale array can be achievable without a cell selector. For details of the simulation, please refer to Supporting Information S2.

CONCLUSIONS

In summary, a double-layer stacked HfO_x vertical RRAM has been demonstrated using a bit-cost-effective fabrication process for the 3D integration. Excellent and consistent switching characteristics of the fabricated devices suggest the potential of stacking even more layers. A TiON interfacial layer is introduced for obtaining nonlinear *I*−*V* curves. As a result, the LRS resistance gets increased at low applied bias for the unselected cells in an array, which is beneficial for a cross-point array without an explicit cell selector. This work paves a technology path toward a 3D cross-point memory architecture with the emerging oxide-based RRAM devices. Future research directions include finding appropriate electrode materials that can replace Pt since Pt is not fully compatible with the CMOS integration process.

METHODS

Device Fabrication. We design a bit-cost-effective fabrication process for potential 3D integration, and the schematic of the process flow is shown in Supporting Information S3: (1) Multilayer stacked Pt (20 nm)/SiO_2 (30 nm) is deposited by e-beam evaporation and low-pressure chemical vapor deposition, respectively; (2) a trench (1−100 μm in size) is dry etched down to the bottom SiO_2 layer; (3) 5 nm HfO_x is deposited by atomic layer deposition, which conformally covers the sidewall of the trench; (4) 150 nm TiN is deposited by reactive sputtering to fill the trench as the pillar electrode; the oxygen ambient is introduced during sputtering to form the TiON interfacial layer; (5) the Pt plane electrode at the edge of the memory cell area is exposed by dry etching so it can be separately contacted electrically. The vertical HfO_x RRAM cells are formed at the sidewall between the TiN pillar electrode and Pt plane electrode. Two types of samples have been fabricated: one is the single-layer sample with one cell on the sidewall per trench; the other is the double-layer sample with two cells on the sidewall per trench.

TEM and Composition Characterization. The TEM-ready samples were prepared using the *in situ* focused ion beam (FIB) lift out technique on an FEI 830 dual beam FIB/SEM. The sample was coated with a protective platinum layer prior to FIB milling. The samples were imaged with a FEI Tecnai TF-20 FEG/TEM operated at 200 kV in bright-field mode, high-resolution mode, and high-angle annular dark-field STEM mode. EDX spectra were obtained in STEM mode using a nominal 3 nm electron beam and an Oxford INCA EDX detector system. The EELS line scan was obtained in STEM mode using a nominal 1 nm electron beam and a Gatan Enfina DigiP EELS spectrometer.

Electrical Measurements. Electrical measurements are performed using a Keithley 4200 semiconductor parameter analyzer and an Agilent 81150A pulse generator. The voltage is applied on the Pt plane electrode, and the TiN pillar electrode is grounded as a reference.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: This section includes the conduction mechanism study of the LRS, the 3D cross-point memory array simulation, and the bit-cost-effective fabrication process for potential 3D integration. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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